

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

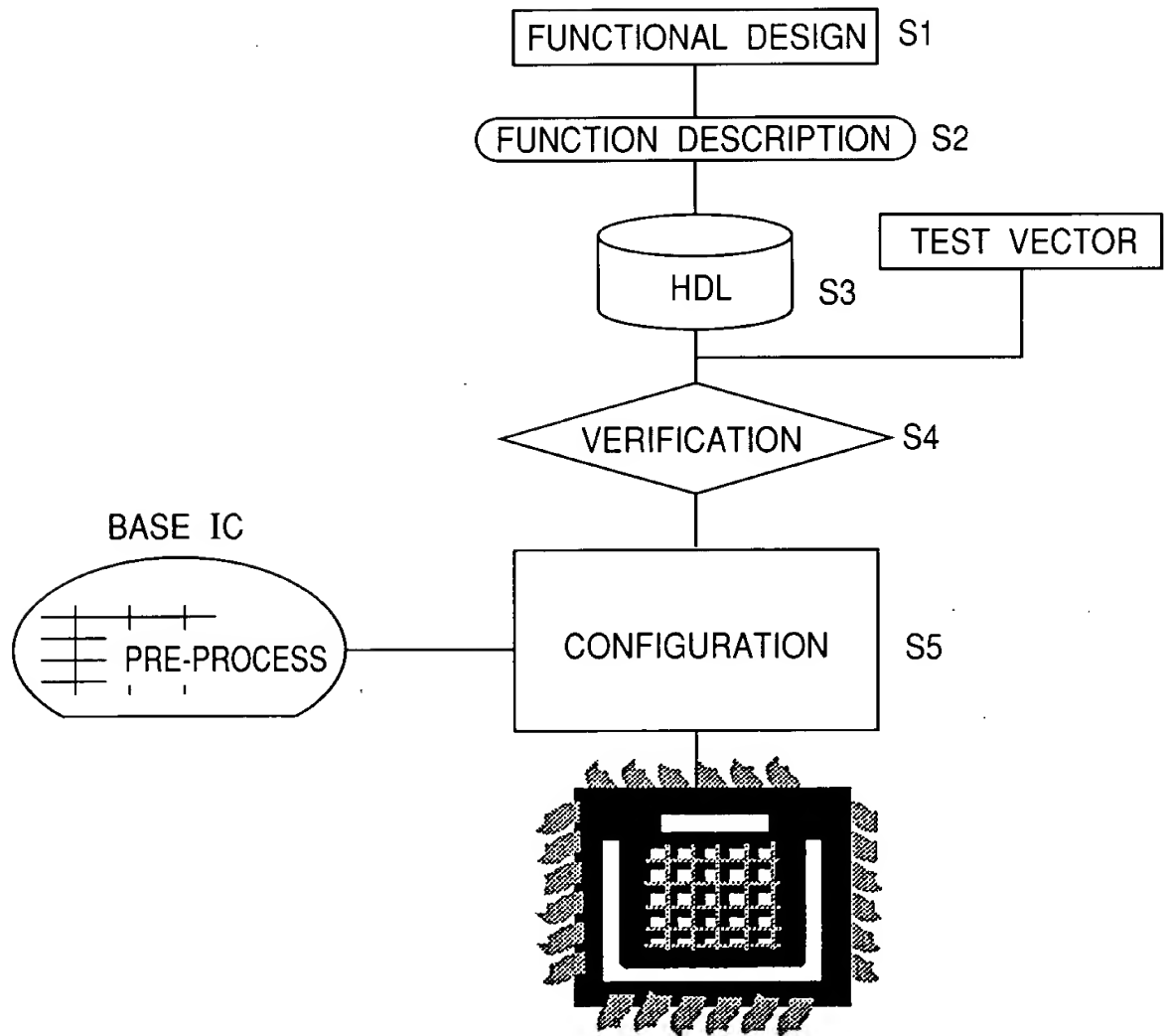
**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

09/914429

1 / 14

FIG. 1

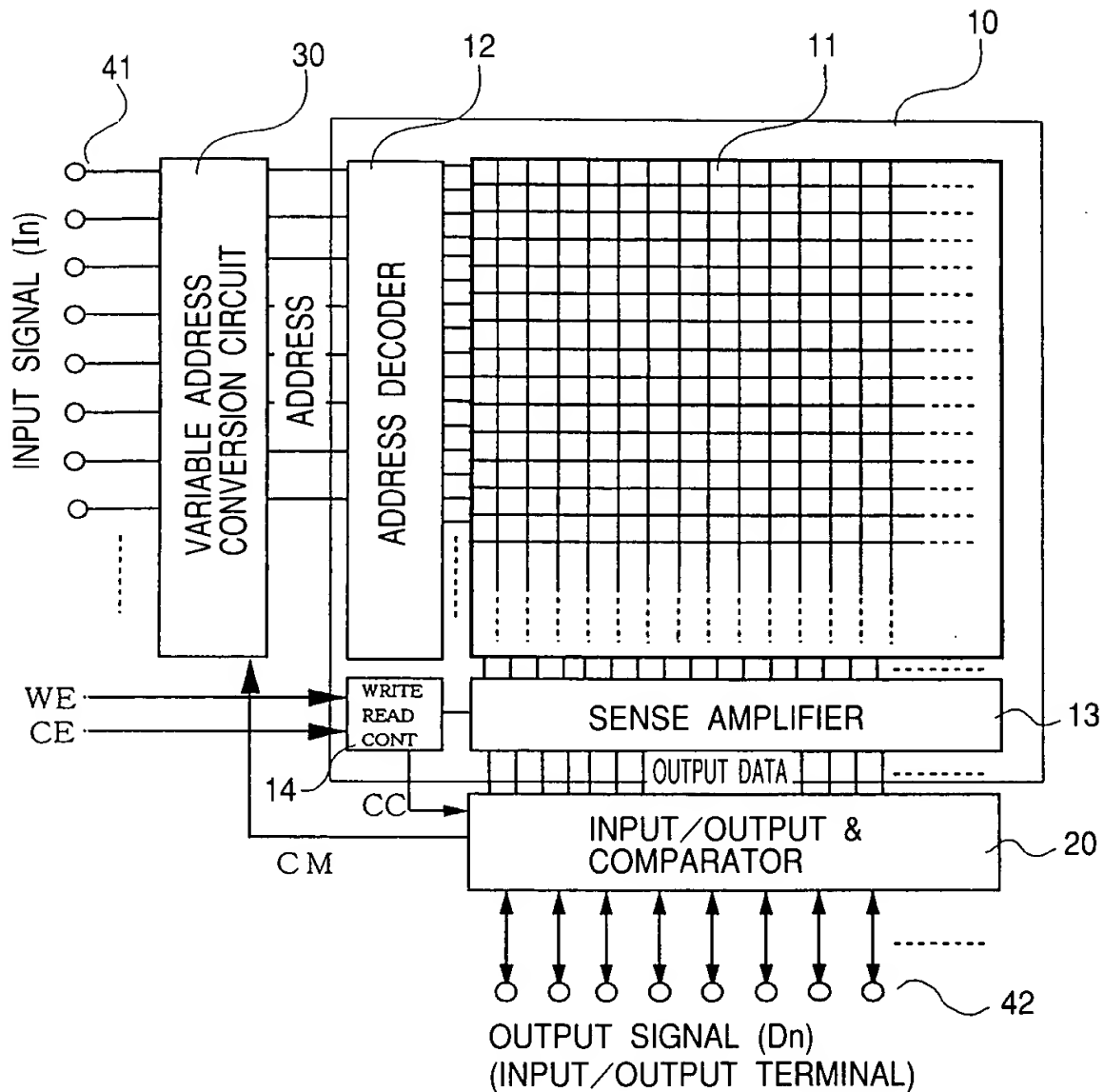


09/914429-110504

2 / 14

09/914429

FIG. 2



09/914429

3 / 14

FIG. 3

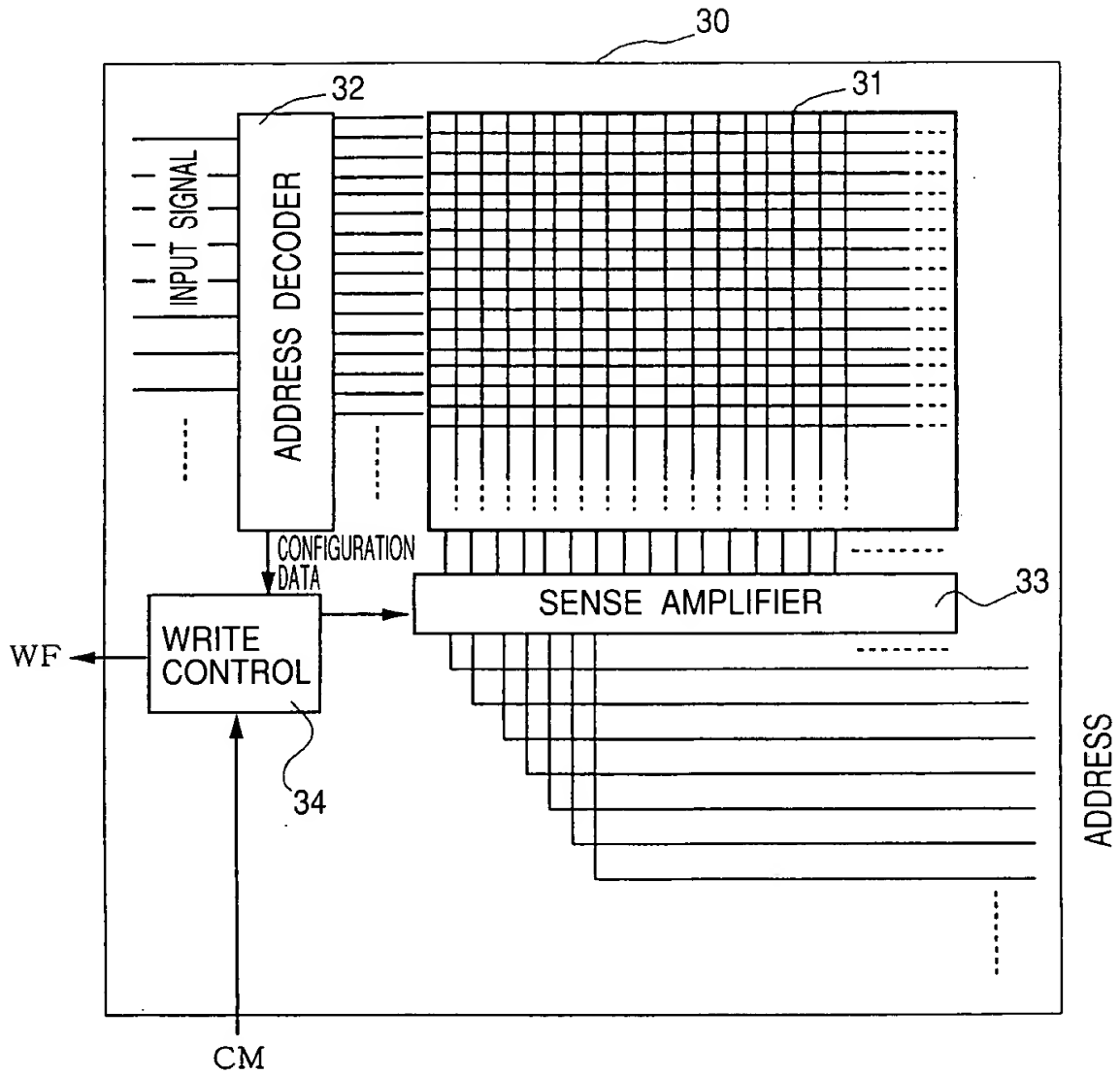
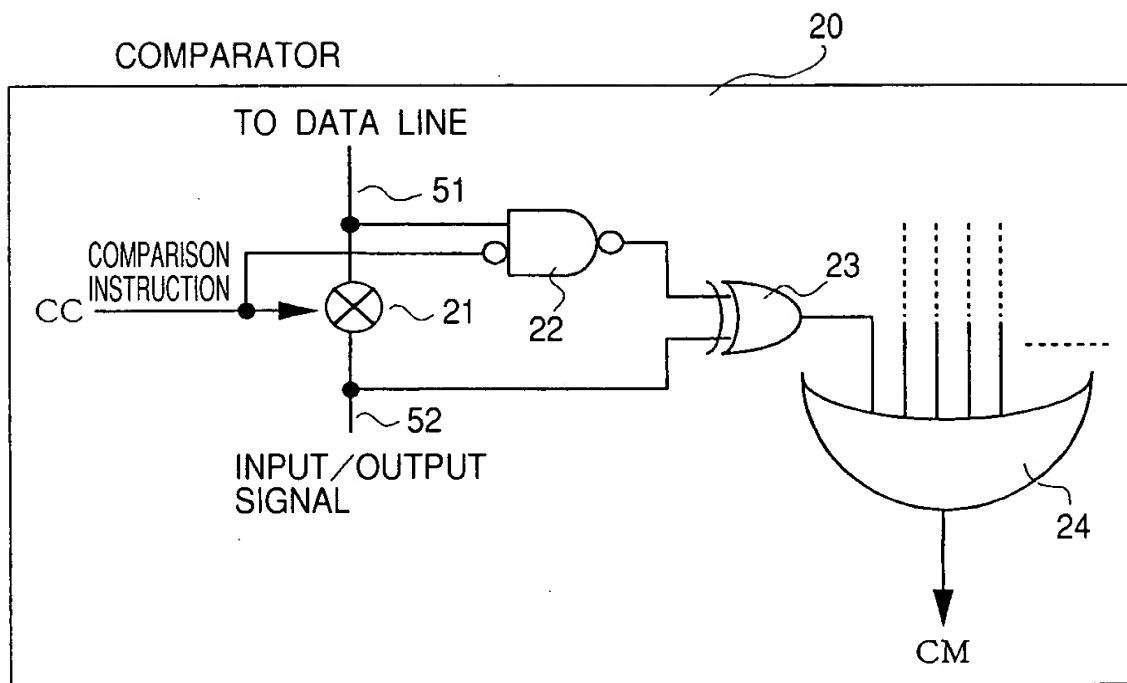
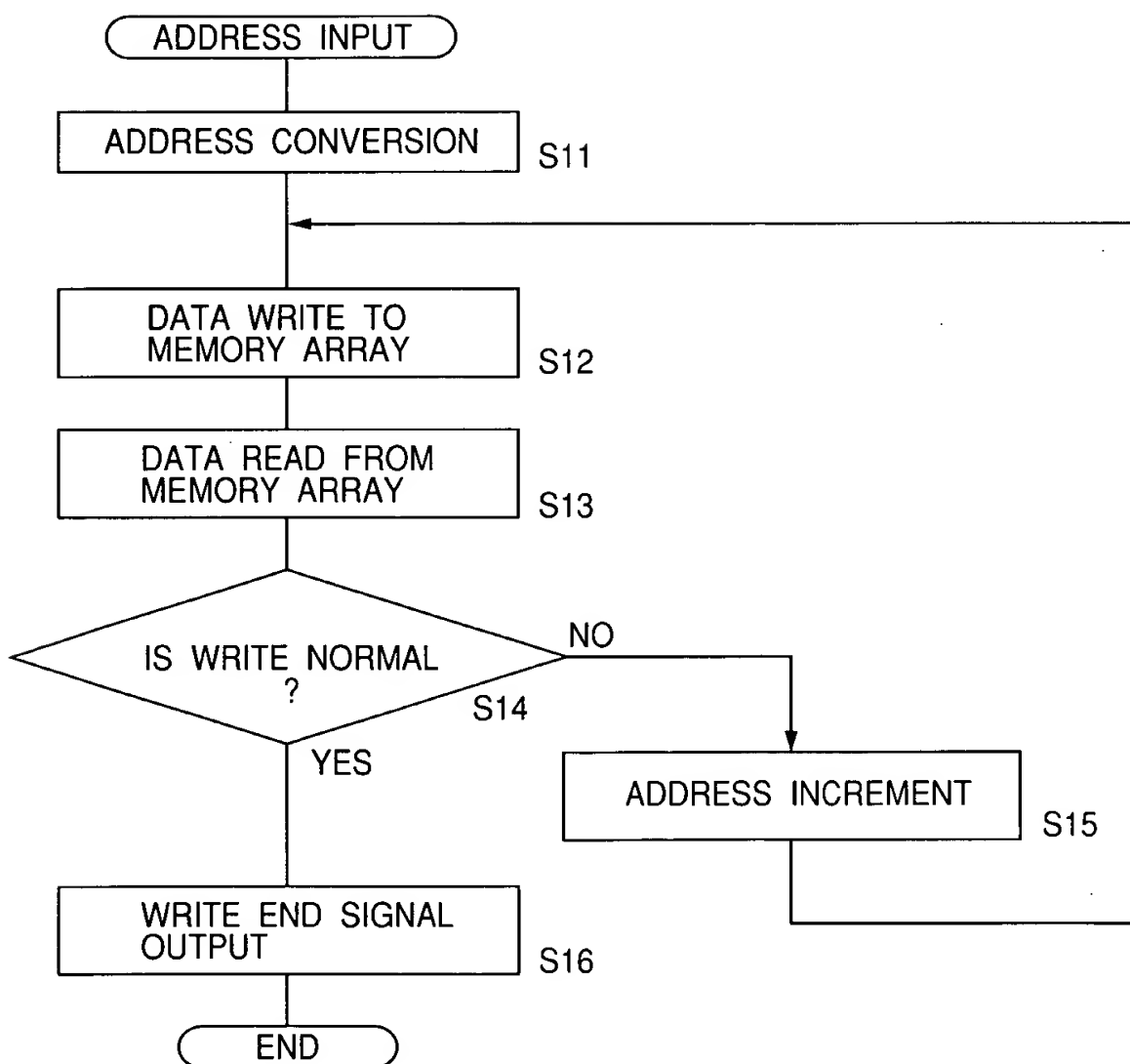


FIG. 4



**FIG. 5**

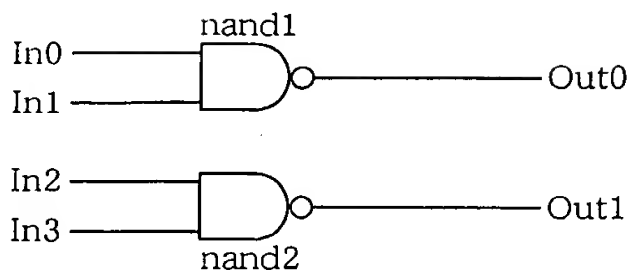


445044 00000000

09/914429

6 / 14

FIG. 6



## HDL DESCRIPTIVE STATEMENT

//External Declaration

module nand1\_gate(

In0,

In1,

Out0

);

//Internal Declarations

input In0;

input In1;

wire In0;

wire In1;

reg Out0;

always @ (In0 or In1) begin

//Block 1

case(In0, In1)

2'b 00:

Out0=1'b1;

2'b 01:

Out0=1'b1;

2'b 10:

Out0=1'b1;

2'b 11:

Out0=1'b0;

default

;

endcase

end

endmodule // nand1\_gate

//External Declaration

module nand2\_gate(

In2,

In3,

Out1);

//Internal Declarations

input In2;

input In3;

wire In2;

wire In3;

reg Out1;

always @ (In2 or In3) begin

//Block 1

case(In2, In3)

2'b 00:

Out1=1'b1;

2'b 01:

Out1=1'b1;

2'b 10:

Out1=1'b1;

2'b 11:

Out1=1'b0;

default

;

endcase

end

endmodule // nand1\_gate2

09/914429-10501

09/914429

7/14

FIG. 7

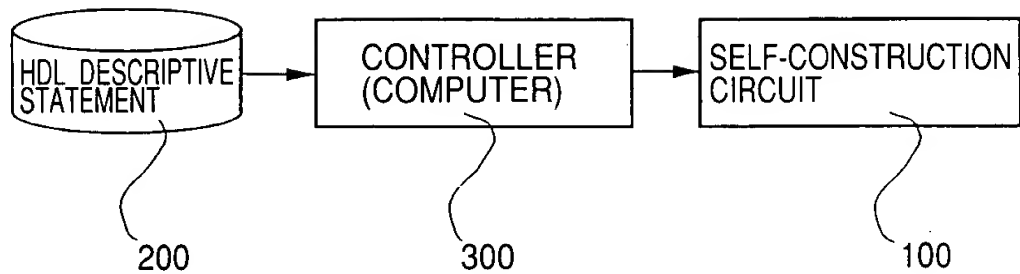
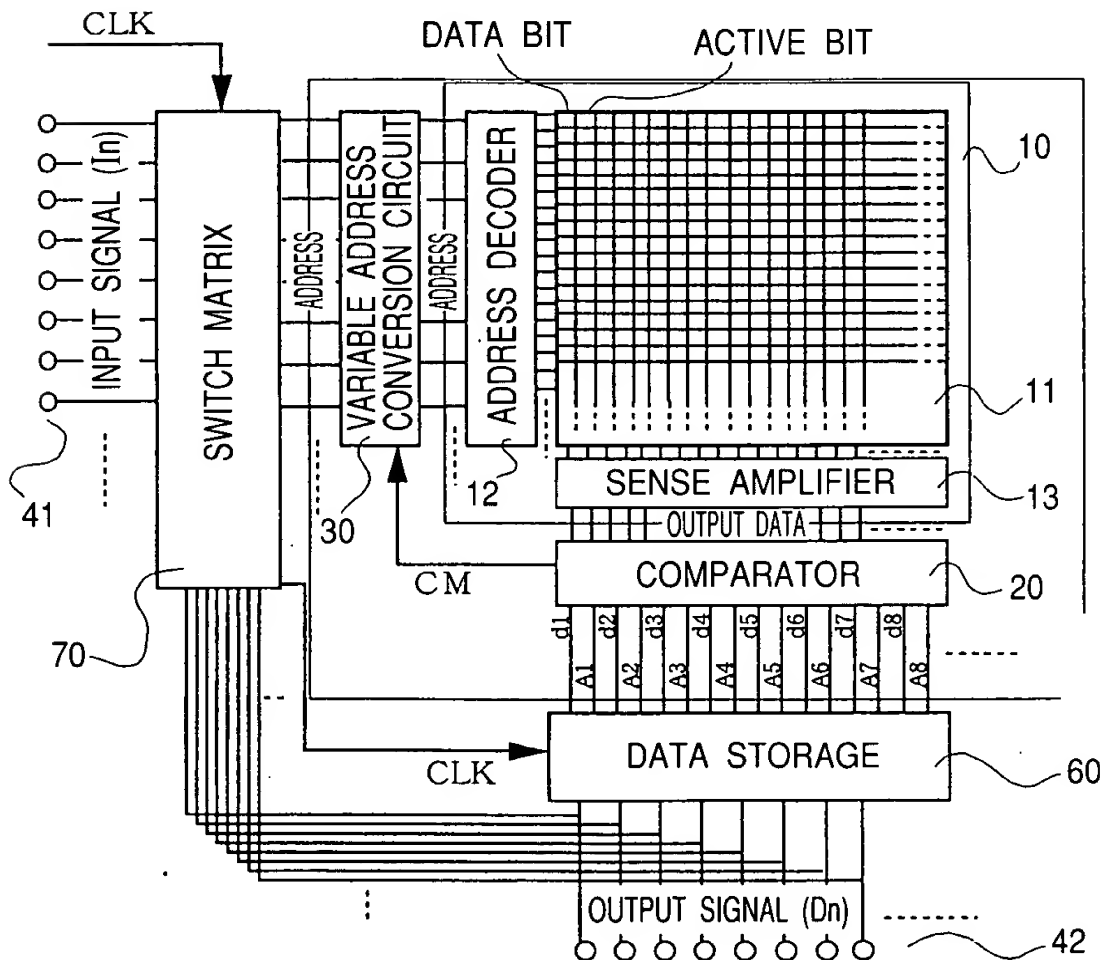


FIG. 8

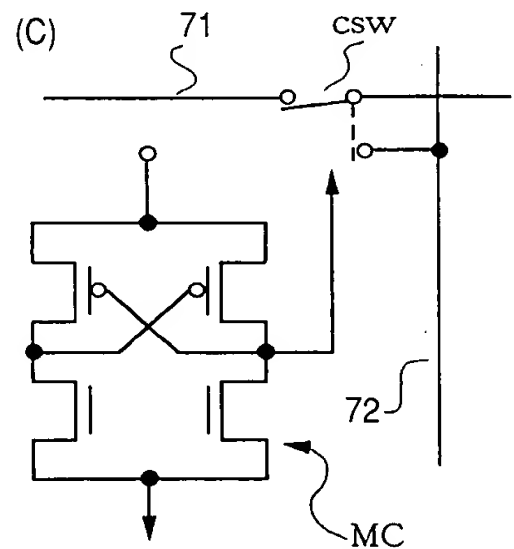
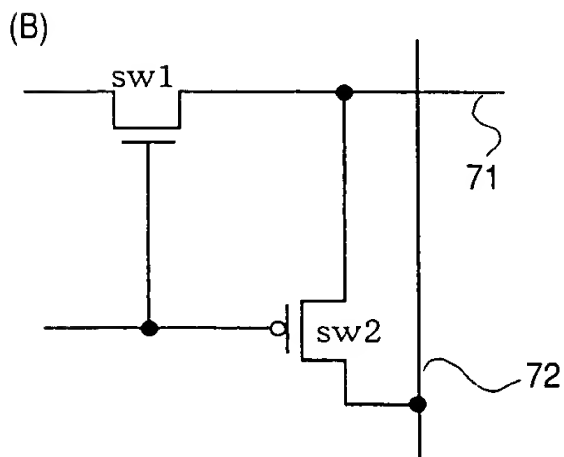
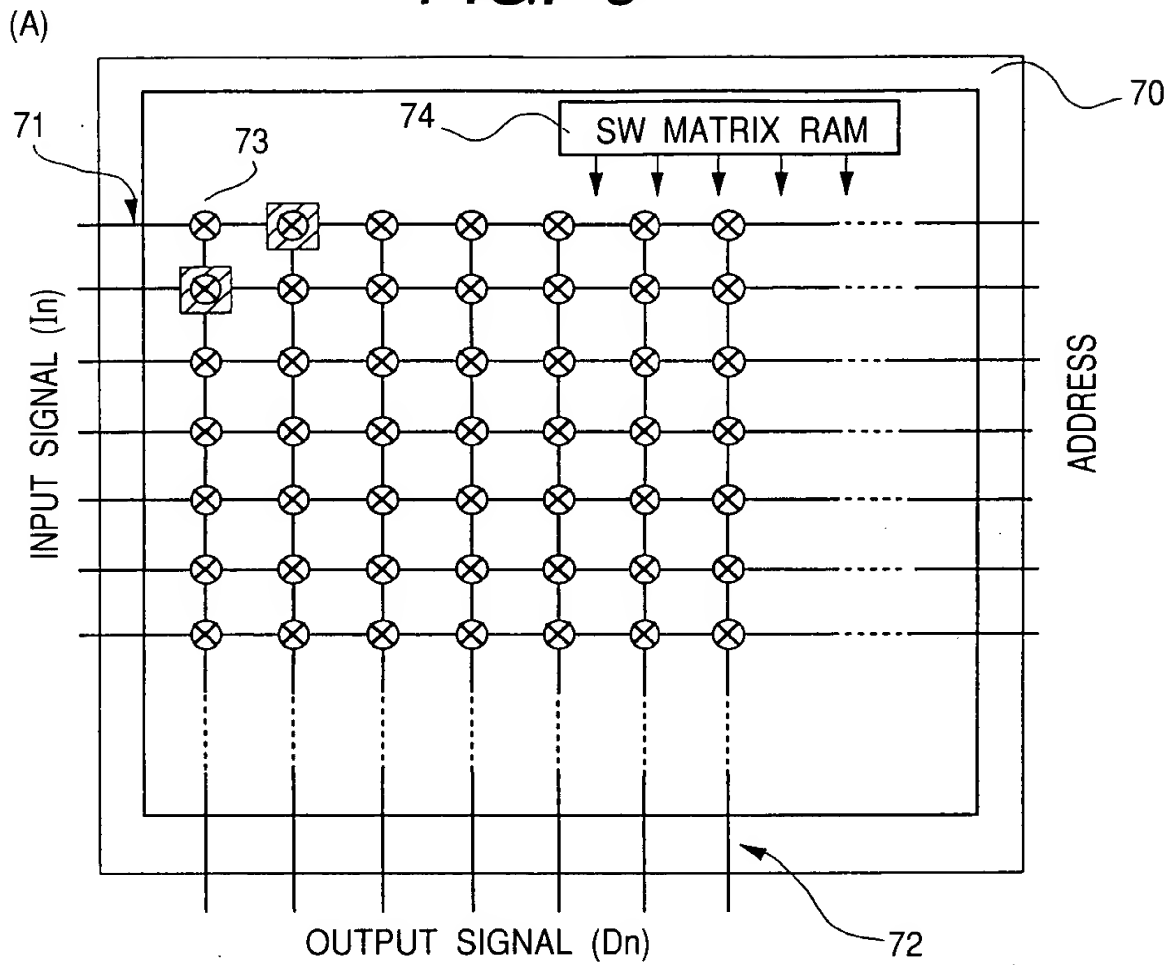




09/914429

8 / 14

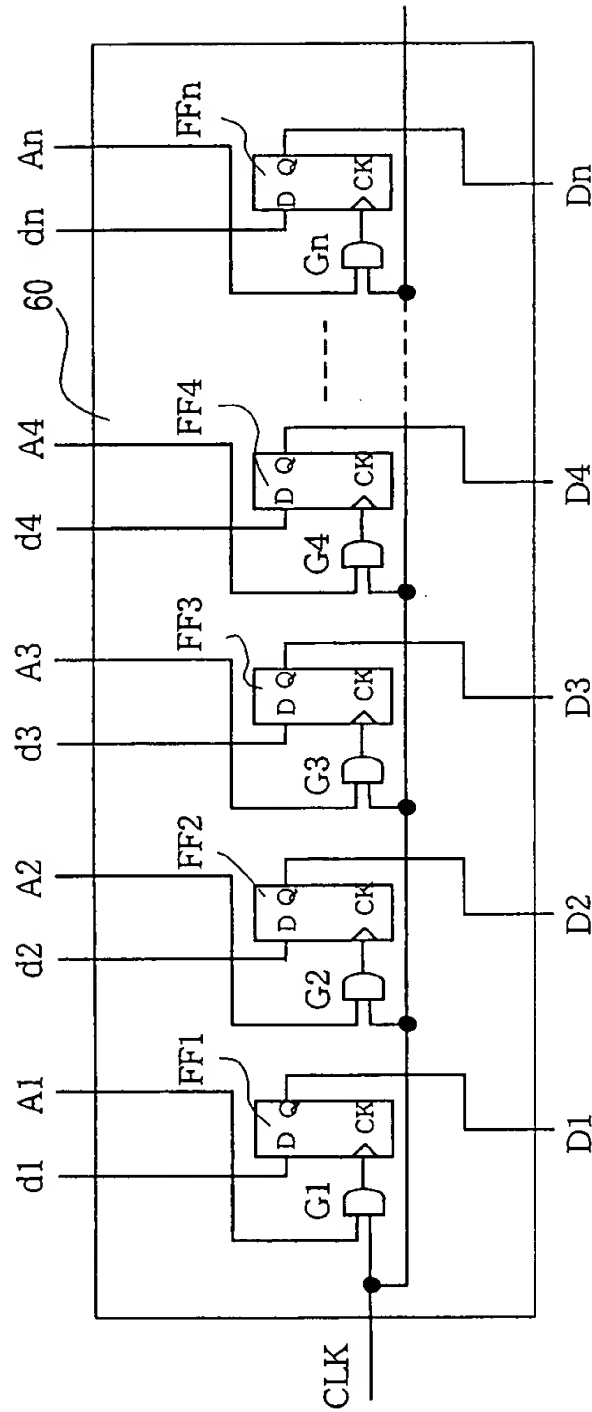
FIG. 9



09/914429

9/14

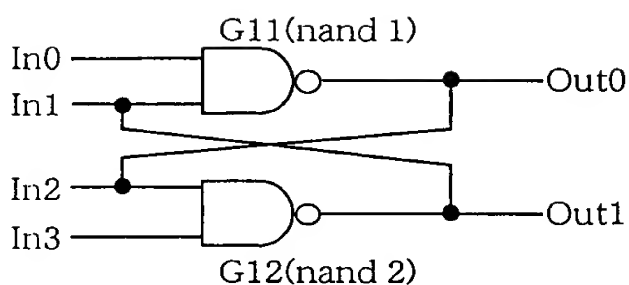
FIG. 10



09/914429

10 / 14

FIG. 11



## HDL DESCRIPTIVE STATEMENT

```

//External Declaration
module ff_model(
    In0,
    In1,
    Out0,
    Out1
);
//Internal Declarations
input In0;
input In1;
output Out0;
output Out1;
wire In0;
wire In1;
reg Out0;
reg Out1;
//Local declarations
//Instaces
nand1_gate(
    .In0(In0),
    .In1(Out1),
    .Out0(Out0),
);
nand2_gate(
    .In2(Out0),
    .In3(In3),
    .Out0(Out1)
);
endmodule // ff_model

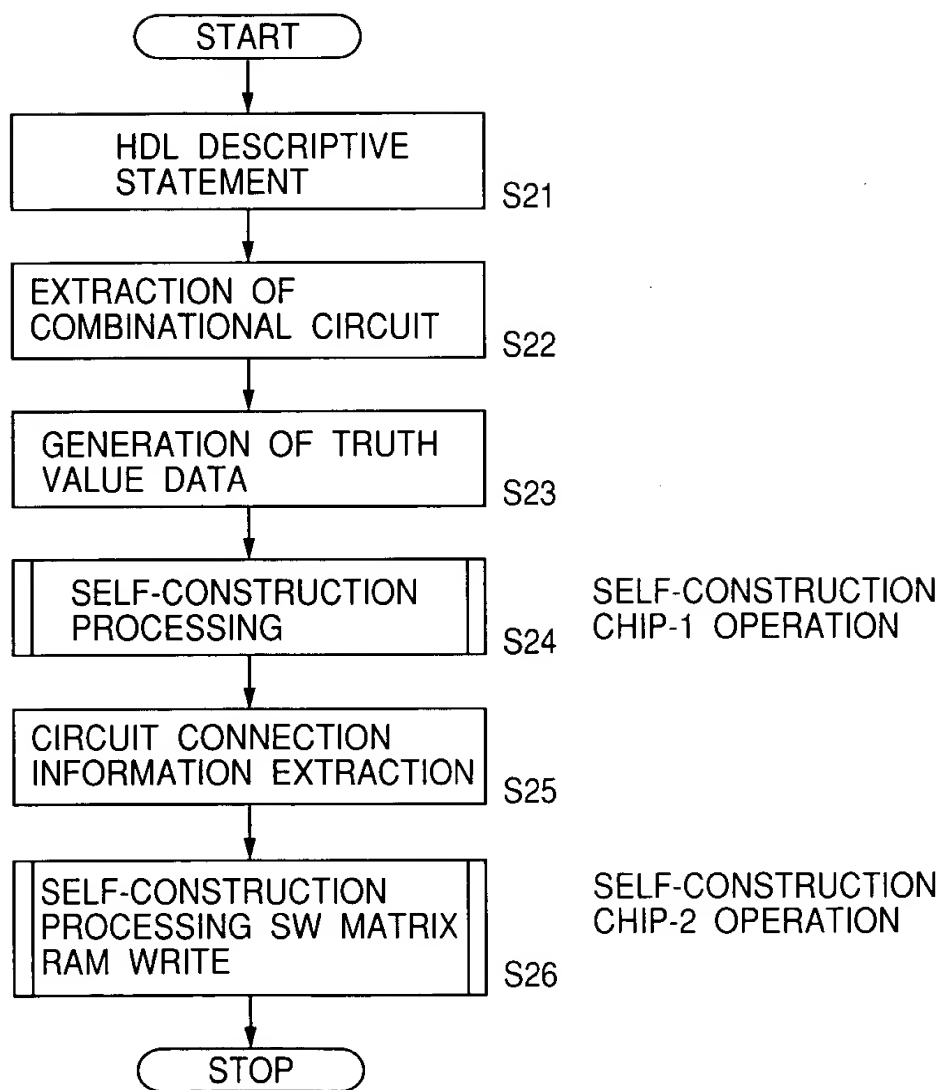
```

FIG. 11: 6244T600

09/914429

11 / 14

FIG. 12

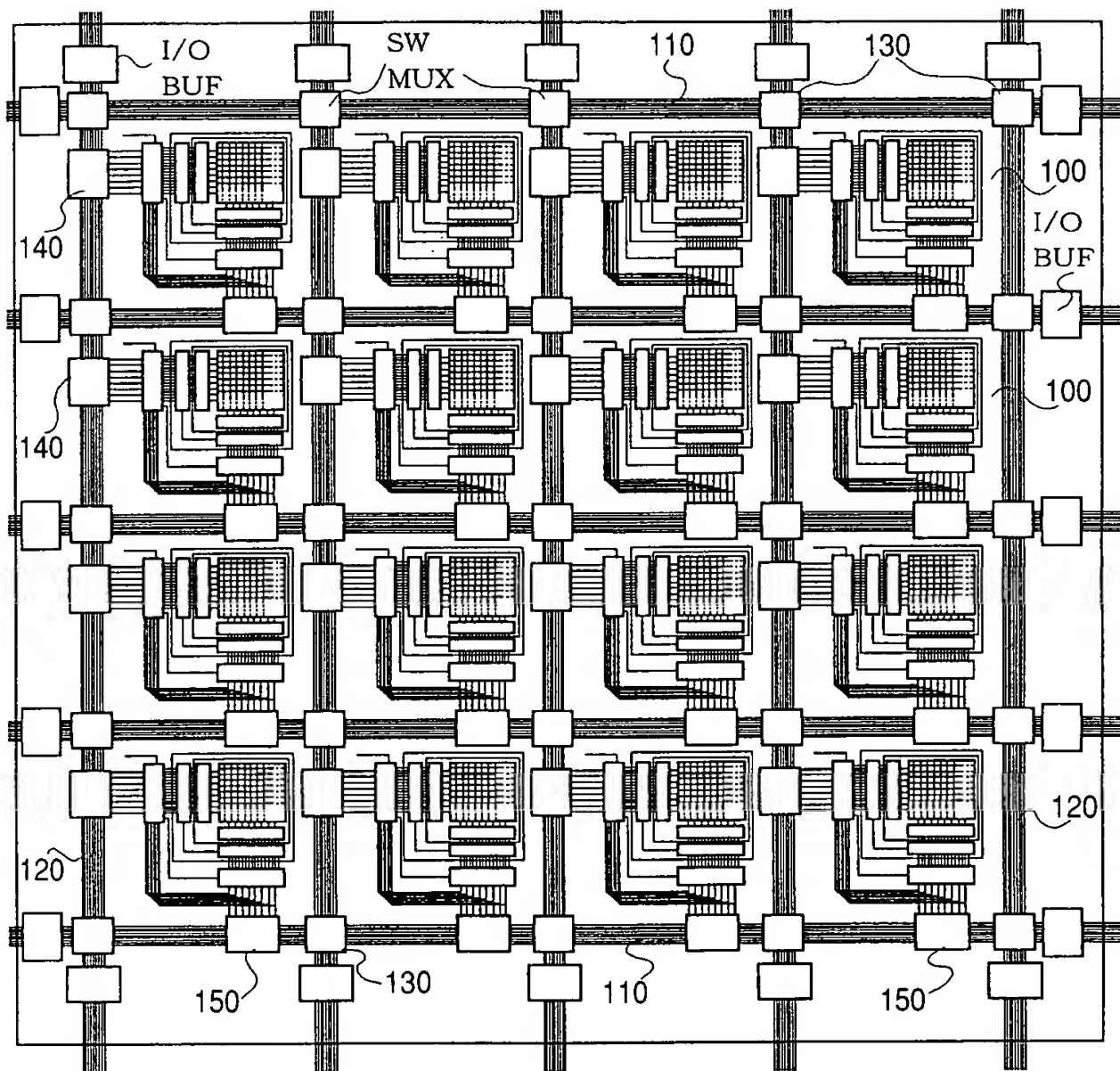


09/914429:10504

09/914429

12/14

FIG. 13

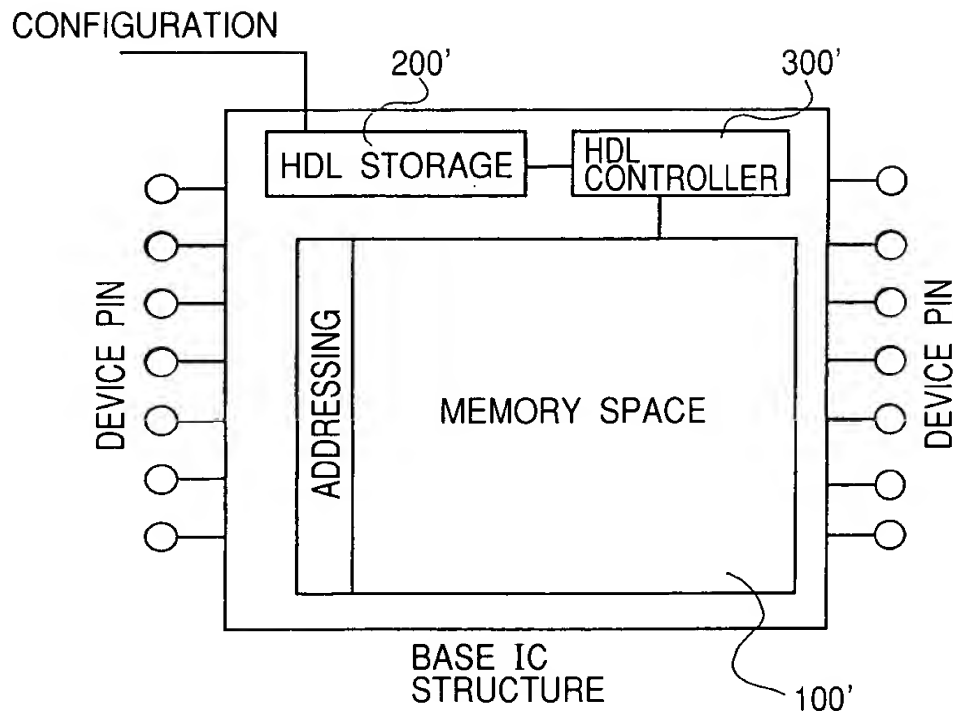


00014429 10501

09/914429

13 / 14

FIG. 14



09/914429-1300

|           |             |
|-----------|-------------|
| DESIGNED  | O.G. FIG.   |
| BY        | CLASS SUBC. |
| CRAFTSMAN |             |

14 / 14

09/914429

**FIG. 15**